27C202
Fast Word-Wide 256K (16K x 16) EPROM

- **High Speed**
  - **— 70 ns Access Time Maximizes CPU Performance**
- **Low-Power CHMOS***
  - **— 100 mA Active, 15 mA Standby**
- **High Drive Capability**
  - **— 4 mA Source/16 mA Sink Handles Large Arrays**
- **High-Density Upgrade Pinout**
  - **— Matches 27210 1M EPROM**
- **Rapid Programming**
  - **— 4 Second Throughput for Automated Manufacturing**
- **Simple Interfacing**
  - **— TTL and CMOS Compatible**
  - **— 2-Line Output Control**
- **Versatile Package Options**
  - **— Standard 40-Pin DIP**
  - **— Compact Surface-Mount 44-Lead PLCC****
  - **— 44-Lead Cerquad**

(See Packaging Spec., Order No. 231369)

The Intel 27C202 is a high-performance, 262,144-bit, electrically programmable read only memory organized as 16 K-words of 16 bits each. Its high-density, word-wide configuration provides high integration for today's speed-critical applications.

The 27C202 meets no-wait-state performance requirements for many advanced 32-bit microprocessors. The large 256 K-bit capacity is well suited for high-end embedded control applications. The 27C202's organization provides an optimal single-chip firmware solution for code needs of monolithic 16-bit digital signal processors. System interfacing is simple, given two-line output control common to all standard Intel EPROMs. In addition, both TTL and CMOS logic can be used with the 27C202.

Three different packages are available for the 27C202. The standard 40-pin Dual-In-Line Package (DIP) provides for conventional device handling and socketing. Also, a 44-lead, One-Time-Programmable (OTP™) Plastic Leaded Chip Carrier (PLCC) allows lowest-cost, automated, surface-mount manufacturing. The 44-lead windowed Cerquad package allows reprogramming with the same compact dimensions as the PLCC package.

The Quick-Pulse Programming™ algorithm, with throughput times as fast as 4 seconds per device, improves manufacturing efficiency.

The 27C202 is manufactured on Intel's advanced CHMOS* III-E process, which is optimized for high-performance products.

The 27C202 will be replaced by the 27C202C mid-1990. The 27C202C will be functionally identical to the 27C202 in the read mode. The 27C202C's memory array will use a 1-transistor cell, versus the 27C202's 2-transistor cell, and will program with a standard one-pass algorithm.

*CHMOS is a patented process of Intel Corporation. **PLCC package availability TBD

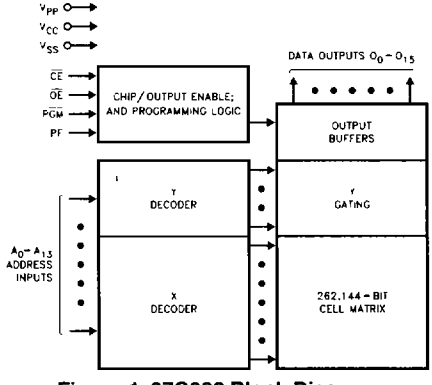


Figure 1. 27C202 Block Diagram

October 1989
Order Number: 290136-006

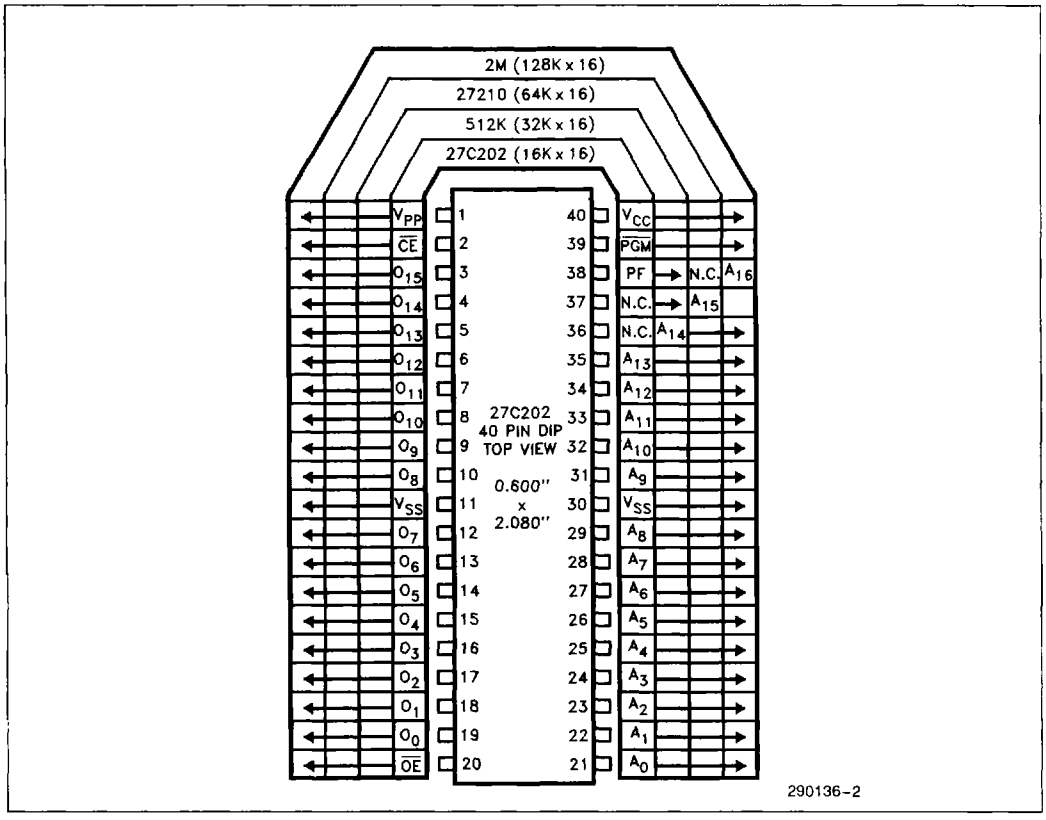


Figure 2. DIP Pin Configurations

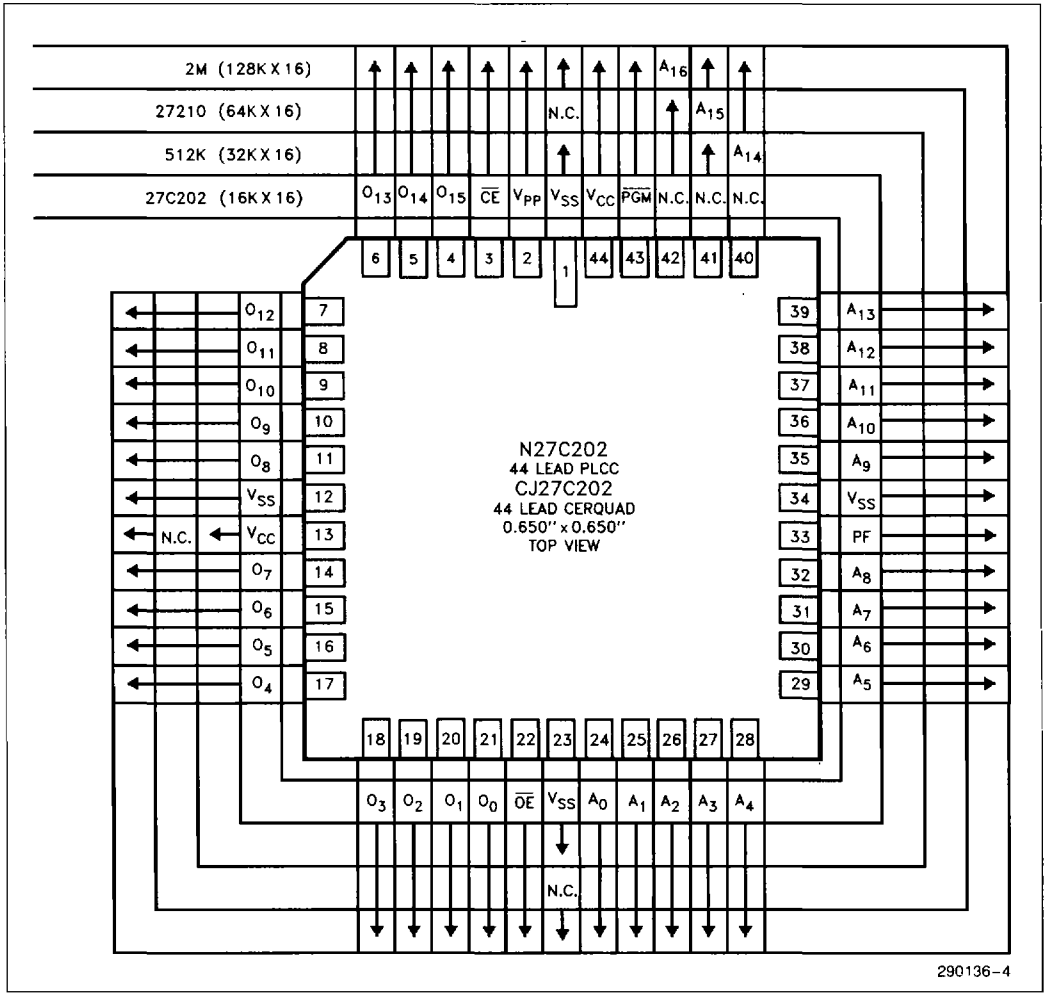


Figure 3. Cerquad/PLCC Lead Configurations**

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
$\overline{PGM}$	Program Enable
PF	Program Function
N.C.	No Connect

*CHMOS is a patented process of Intel Corporation.

NOTES:
1. Upgrade paths to higher densities are shown next to 27C202 pinouts.
2. Each 27C202 V_{CC} and V_{SS} pin specified must be tied individually to their respective power supplies. See System Design Considerations.

**Cerquad is available in a socket only version until the third quarter of 1990.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read . 0°C to +70°C
Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... −2V to +7V(1)
Voltage on A_9 with Respect to Ground ..... −2V to +14V(1)
V_{PP} Supply Voltage with Respect to Ground During Programming .... −2V to +14V(1)
V_{CC} Supply Voltage with Respect to Ground ..... −2V to +7.0V(1)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Conditions
		Min	Max	Units	
I_{LI}	Input Load Current		10	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = 5.5V$
I_{PP1}	V_{PP} Load Current Read		10	µA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby		15	mA	$\overline{CE} = V_{IH}$
I_{CC}(2)	V_{CC} Current Active		100	mA	$\overline{CE} = OE = V_{IL}$
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 16$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -4$ mA

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

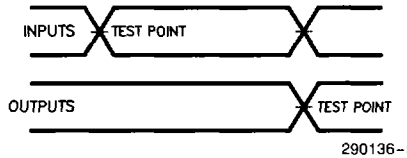
Versions(3)	$V_{CC} \pm 5\%$ (5.0 ±0.25V)	C27C202-70V05 CJ27C202-70V05		C27C202-90V05 CJ27C202-90V05		Units
	$V_{CC} \pm 10\%$ (5.0 ±0.50V)	C27C202-70V10 CJ27C202-70V10		C27C202-90V10 CJ27C202-90V10		
Symbol	Characteristics	Min	Max	Min	Max	
t_{ACC}(5)	Address to Output Delay		70		90	ns
t_{CE}(5)	$\overline{CE}$ to Output Delay		70		90	ns
t_{OE}(5)	$\overline{OE}$ to Output Delay		30		35	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	15	0	20	ns
t_{OH}(4)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		ns

NOTES:
1. Specified D.C. input voltage ranges are shown in the D.C. Read and D.C. Program Characteristics tables. Absolute maximum input voltages apply to overshoot durations of 20 ns or less; otherwise device damage may occur.
2. V_{CC} current assumes no output loading, i.e., $I_{OH} = I_{OL} = 0$ mA.
3. Packaging Options: C = Ceramic Side-Brazed DIP, CJ = Cerquad.
4. *This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven.*
5. A derating factor of 6 ns/100 pF should be used with output loading greater than 30 pF. This derating factor is only sampled and not 100% tested.

CAPACITANCE[1] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	12	15	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	15	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Input Capacitance		75	pF	V_{PP} = 0V

A.C. TESTING INPUT/OUTPUT WAVEFORM



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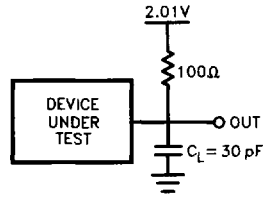
A.C. Testing inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Timing measurements are made at 1.5V for both Logic "1" and Logic "0" output levels. Rise and fall times are 5 ns.

A.C. TESTING LOAD CIRCUIT



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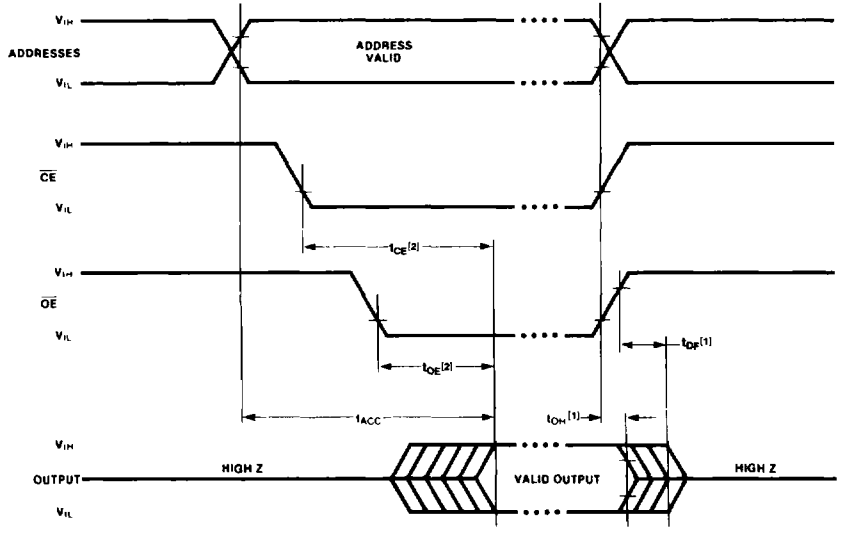
C_L = 30 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



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NOTES:
1. These parameters are only sampled and are not 100% tested.
2. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

Table 1 shows 27C202 operating modes. All inputs are TTL levels indicated in DC Characteristics unless otherwise specified.

Table 1. Mode Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	PF	A_9	A_0	Outputs	V_{CC}	V_{PP}
Read		V_{IL}	V_{IL}	X	X	A_9	A_0	D_{OUT}	V_{CC} Read	V_{CC} Read
Standby		V_{IH}	X	X	X	X	X	High Z	V_{CC} Read	V_{CC} Read
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z	V_{CC} Read	V_{CC} Read
int$_e$ligent Identifier	Manufacturer	V_{IL}	V_{IL}	X	X	V_H	V_{IL}	0089 H	V_{CC} Read	V_{CC} Read
	Device	V_{IL}	V_{IL}	X	X	V_H	V_{IH}	66FE H		
Blank Checks	Ones	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A_9	A_0	Zeros	V_{CC} Program	V_{PP}
	Zeros	V_{IL}	V_{IL}	V_{IH}	V_{IL}	A_9	A_0	Ones		
Program Verify	Ones	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A_9	A_0	Ones	V_{CC} Program	V_{PP}
	Zeros	V_{IL}	V_{IL}	V_{IH}	V_{IL}	A_9	A_0	Zeros		
Program	Ones	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A_9	A_0	D_{IN}	V_{CC} Program	V_{PP}
	Zeros	V_{IL}	V_{IH}	V_{IL}	V_{IL}	A_9	A_0			
Program Inhibit		V_{IH}	X	X	X	X	X	High Z	V_{CC} Program	V_{PP}

READ MODE

A 27C202 has two control functions; both must be logically active to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and the device-select. Output Enable ($\overline{OE}$) gates data to the output pins by controlling the output buffer.

The 27C202 operates asynchronously. Data is valid within the address access time (t_{ACC}) after address inputs are stable on selected devices ($\overline{CE}$ low). If $\overline{CE}$ is activated after the addresses are stable, data is valid within the chip enable access time (t_{CE}). Outputs display valid data t_{OE} after the falling edge of $\overline{OE}$, assuming t_{ACC} and t_{CE} times are met.

STANDBY MODE

The standby mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the standby mode places the outputs in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two line control provides for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory-array devices and the system READ control line. This assures that only selected memory devices have active outputs while deselected devices are in low-power standby mode.

SYSTEM DESIGN CONSIDERATIONS

The 27C202 is a high performance memory with exceptionally strong output drive capability for fast output response. Input levels are sensitive to power supply stability. Special considerations must be given to the large supply current swings associated with switching 16 powerful output drivers. Minimizing

power supply inductance is critical. Wide, short traces with low inductance must be connected from the circuit board's ground and V_{CC} plane to each device. V_{CC} transients must be suppressed with high-frequency 0.1 μF capacitors. Where the solid ground plane of a multilayer board is not available, bulk electrolytic capacitors (typically 4.7 μF) should decouple the V_{CC} and the ground supplies for each group of four 27C202 devices.

The 30 pF load capacitance specified in the A.C. Test Conditions is not a system design limitation. The 27C202 has the output drive capability to handle the capacitive loading of large memory arrays. However, access times must be appropriately derated for loading in excess of 30 pF. T_{ACC}, T_{OE} and T_{CE} should be derated 6 ns/100 pF with output loading greater than 30 pF.

PROGRAMMING MODE

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

To minimize data access time delays, the 27C202 utilizes a 2-transistor cell with differential sensing. The 2-transistor cells are partitioned into "ONES" and "ZEROS" arrays. Programming is done in two passes; once in the "ONES" half of the memory array and once in the "ZEROS" half. The same data word must be presented to the device in both passes. A program function (PF) pin is provided to control this partitioning (see Figure 5).

The programming mode is entered when V_{PP} and V_{CC} are raised to their programming voltages (see Table 2), $\overline{CE}$ and $\overline{PGM}$ are at TTL-low and $\overline{OE}$ = V_{IH}. The data to be programmed is applied 16 bits in parallel to the data output pins. TTL levels are required for the address and data inputs.

PROGRAM INHIBIT

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{PGM}$ or $\overline{CE}$ prevents devices from being programmed.

Except for $\overline{CE}$, all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input, with V_{PP} at programming voltage, $\overline{CE}$ at a TTL-low level, and $\overline{OE}$ at V_{IH} will program the selected device.

PROGRAM VERIFY/BLANK CHECK

The program verify/blank check mode is activated when the $\overline{OE}$ is at a TTL-low level, V_{PP} and V_{CC} are at their programming levels, and the program control line ($\overline{PGM}$) is at a TTL-high level. Blank Check individually confirms unprogrammed status of both arrays **(a blank check cannot be done with a normal read operation with the 2-transistor cell).** Program verify is used to check programmed status. The elevated V_{CC} voltage used during Program Verify ensures high programming margins and long-term data retention with maximum noise immunity.

The program/verify cycle begins with the "ONES" array; the Program Function pin (PF) is held at a TTL-high level. The "ONES" programming is completed when the desired "ONES" bits are verified changed from their unprogrammed state ("ZEROS").

Programming is not complete, however, until the "ZEROS" array program/verify cycle is also finished. The "ZEROS" cycle begins when PF is brought to a TTL-low level. The "ZEROS" programming is completed when the desired "ZEROS" bits are verified changed from their unprogrammed state ("ONES").

Quick-Pulse Programming™ OPERATIONS

The Quick-Pulse Programming™ algorithm is used to program Intel's 27C202. Developed to reduce substantially production programming throughput time, this algorithm can program a 27C202 in under four seconds. Actual programming time depends on the PROM programmer used.

The Quick-Pulse Programming algorithm uses a 100 microsecond initial-pulse followed by a word verification to determine when the addressed word is correctly programmed. The algorithm terminates if 25 100 μs pulses fail to program a word. This is repeated for both the "ONES" and "ZEROS" programming. Figure 5 shows the 27C202 Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/word-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. When programming is complete, all words should be compared to the original data in a standard read mode with V_{CC} = 5.0V.

int$_e$ligent Identifier™ MODE

The int$_e$ligent Identifier™ Mode will determine an EPROM's manufacturer and device type. Programming equipment can automatically match a device with its proper programming algorithm.

The Identifier mode is activated when A9 is at high voltage (V_H). A0 determines the information being accessed. The first address (A0 = V_{IL}) accesses the manufacturer code and the second (A0 = V_{IH}) accesses the device code.

ERASURE CHARACTERISTICS (FOR UV-WINDOW PACKAGES)

Light with wavelengths shorter than 4000 Angstroms (Å) causes EPROM erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000–4000 Å range. Constant exposure to room-level fluorescent light can erase an EPROM in about 3 years while direct sunlight erasure occurs within approximately 1 week. Covering windowed EPROMs with opaque labels prevents such unintended erasure.

The recommended erasure procedure is to expose the EPROM to a 2537 Å ultraviolet (UV) source for a minimum integrated dose (intensity × exposure time) of 15 W-sec/cm^2. The EPROM should be placed within 1 inch of the light source and will erase in 15 to 20 minutes with a typical 12000 μW/cm^2 lamp.

Overexposure to high-intensity UV light can cause permanent device damage. The maximum integrated dose allowed is 7258 W-sec/cm^2 (approximately 1 week at 12000 μW/cm^2).

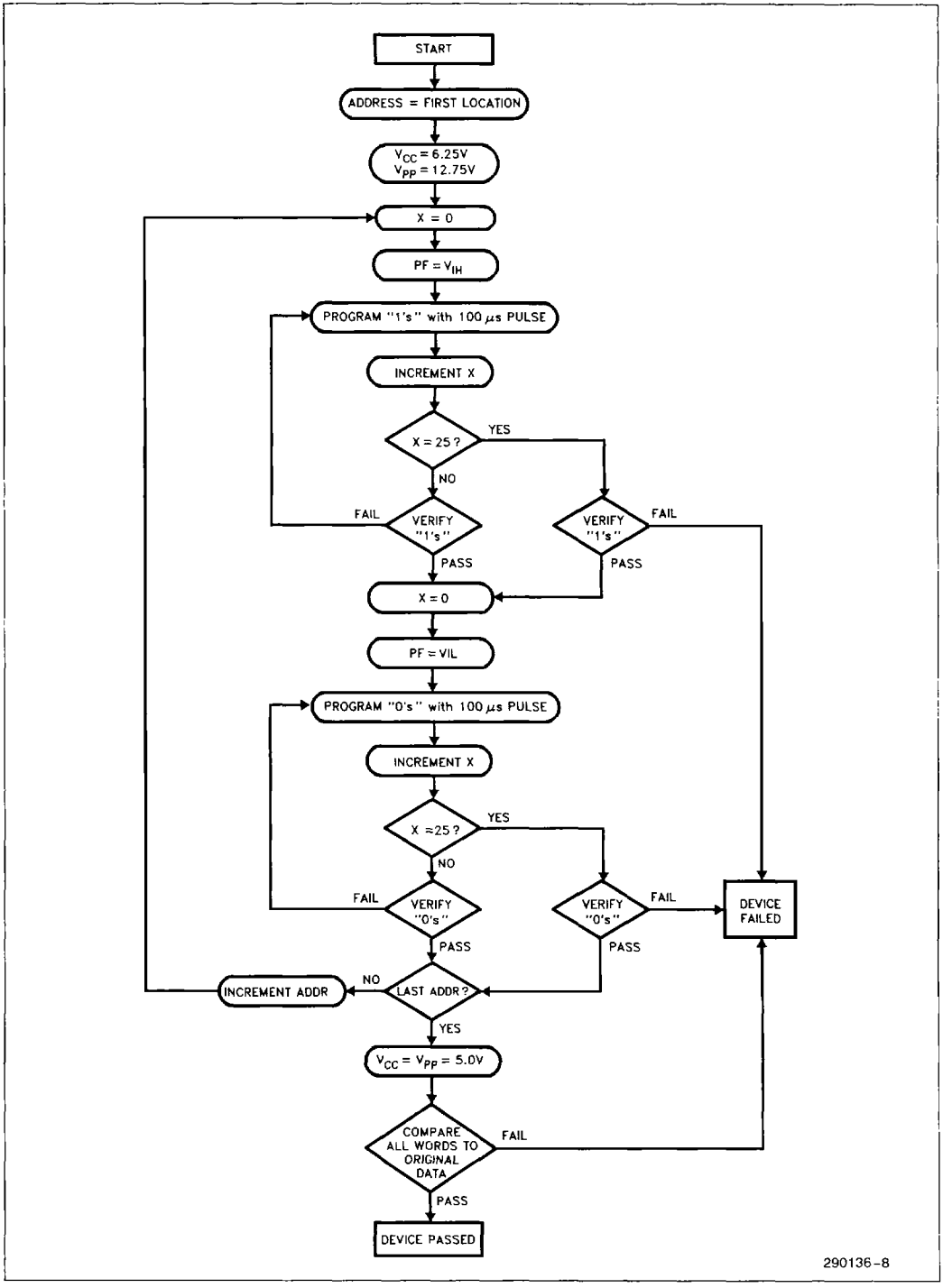


Figure 4. 27C202 Programming Algorithm

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{LI}	Input Leakage Current (All Inputs)		10	μA	$V_{IN} = 6V$
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.4	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 16$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -4$ mA
I_{CC2}(2)	V_{CC} Supply Current (Program & Verify)		100	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{ID}	A9 intelligent Identifier Voltage	11.5	12.5	V	$V_{CC} = 5V$
V_{PP}	V_{PP} Supply Voltage	12.5	13.0	V	
V_{CC}	V_{CC} Supply Voltage	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5\%$ (See DC Programming Characteristics for V_{CC} and V_{PP} voltages.)

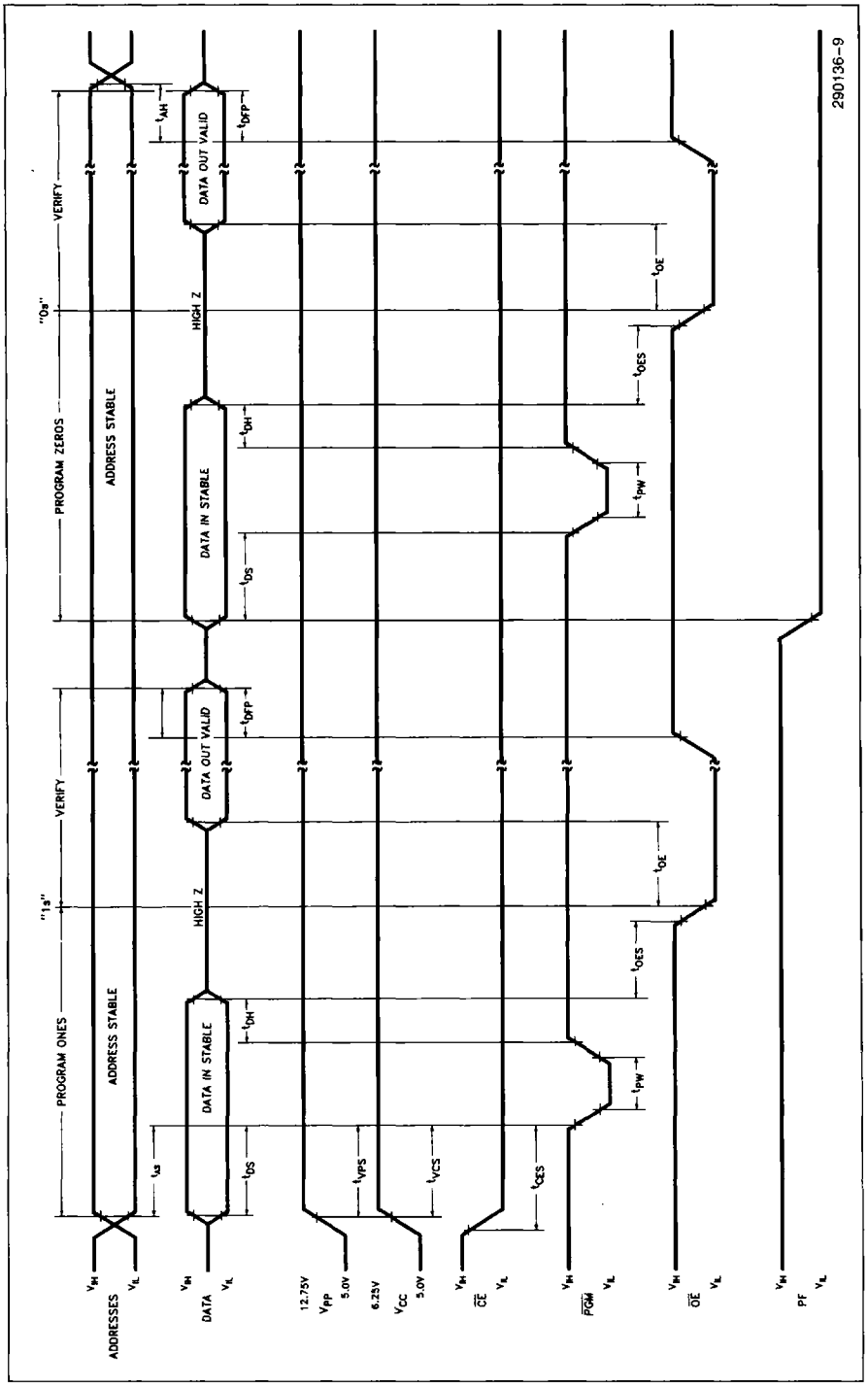
Symbol	Parameter	Limits				Conditions*
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	1			μs	
t_{OES}	$\overline{OE}$ Setup Time	1			μs	
t_{DS}	Data Setup Time	1			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	1			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		50	ns	(Note 1)
t_{VPS}	V_{PP} Setup Time	1			μs	
t_{VCS}	V_{CC} Setup Time	1			μs	
t_{CES}	$\overline{CE}$ Setup Time	1			μs	
t_{PW}	$\overline{PGM}$ Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			35	ns	

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
2. The maximum current value is with outputs O_0–O_{15} unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.